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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,252	TONIETTO ET AL.	
	Examiner	Art Unit	
	Rahel Guarino	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *8,19-21,37-39 and 41-47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to communication filed on 10/14/2008.

Because all claims previously withdrawn from consideration under 37 CFR 1.142 have been rejoined, the restriction requirement as set forth in the Office action mailed on 6/18/2008 is hereby withdrawn. In view of the withdrawal of the restriction requirement as to the rejoined inventions, applicant(s) are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Drawings

2. **Figures 1- 3** should be designated by a legend such as --**Prior Art**-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

3. **Claims 22-32 are** rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. Supreme Court precedent[1] and recent Federal Circuit decisions[2] indicate that a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing. While the instant claim(s) recite a series of steps or acts to be performed, the claim(s) neither transform underlying subject matter nor positively tie to another statutory category that accomplishes the claimed method steps, and therefore do not qualify as a statutory process.

4. Claims 23-32 are rejected to as being dependent upon a rejected base claim.

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[1] *Diamond v. Diehr*, 450 U.S. 175, 184 (1981); *Parker v. Flook*, 437 U.S. 584, 588 n.9 (1978); *Gottschalk v. Benson*, 409 U.S. 63, 70 (1972); *Cochrane v. Deener*, 94 U.S. 780, 787-88 (1876).
[2] *In re Bilski*, 88 USPQ2d 1385 (Fed. Cir. 2008).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3,7,9,10,22,23,33,34,40 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriuchi US 6,556,637

Re claim 1, Moriuchi discloses an integrated decision feedback equalizer and clock and data recovery circuit, comprising (fig.4): a decision feedback equalizer (34, col. 4 lines 30-32); a clock recovery circuit (37, col. 4 lines 41-45); and a flip-flop (fig. 7 of 44) that comprises a portion of both the decision feedback equalizer and the clock recovery circuit (fig.7; col. 4 lines 63-67).

Re claim 2, the integrated decision feedback equalizer and clock and data recovery circuit of claim 1 wherein: the decision feedback equalizer generates a binary data signal (a(n); col. 4 lines 63-64); the clock recovery circuit generates an extracted clock signal (col. 4 lines 65-66); the flip-flop is coupled to receive the binary data signal (a(an)) and the extracted clock signal (b(n)) to generate a flip-flop output signal (col. 6 lines 31-32); and the flip-flop output signal is provided to the decision feedback

equalizer to provide a first feedback signal (S1) and is provided to the clock recovery circuit to provide a first phase detector signal (col. 6 lines 53-55).

Re claim 3, the integrated decision feedback equalizer and clock and data recovery circuit of claim 2, comprising a plurality of latches coupled to receive the flip-flop output signal to generate latch output signals (col. 7 lines 2-4), wherein the latch output signals comprise at least one second feedback signal for the decision feedback equalizer and second phase detector signals for the clock recovery circuit (col. 7 lines 4-10).

Re claim 7, the integrated decision feedback equalizer and clock and data recovery circuit of claim 2 wherein the decision feedback equalizer comprises: a multiplier (67) coupled to receive the flip-flop output signal to generate a scaled feedback signal; a summer (66) coupled to receive an input data signal and the scaled feedback signal to generate a soft decision data signal; and a slicer (43) coupled to receive the soft decision data signal to generate the binary data signal (col. 7 lines 2-10).

Re claim 9, the integrated decision feedback equalizer and clock and data recovery circuit of claim 2 wherein the flip-flop output signal comprises a recovered data signal (col. 4 lines 63-67).

Re claim 10, the integrated decision feedback equalizer and clock and data recovery circuit of claim 3 wherein one of the latch output signals comprises a recovered data signal (col. 4 lines 63-67).

Re claim 22, Moriuchi discloses a method of recovering data from a received data signal, comprising: summing (fig.4(42)) a received data signal and at least one scaled feedback signal to generate a soft decision data signal (col. 2 lines 51-53); digitizing the soft decision data signal to generate a binary data signal (col. 2 lines 53-55); generating a first output signal by clocking the binary data signal into a flip-flop using an extracted clock signal (col. 4 lines 63-67); generating a second output signal by clocking the first output signal into a first latch using the extracted clock signal; generating a third output signal by clocking the second output signal into a second latch using the extracted clock signal (col. 6 lines 24-28); generating the at least one scaled feedback signal by multiplying the first output signal by a first equalization coefficient (col. 7 lines 2-10); and generating the extracted clock signal according to the binary data signal, the first output signal, the second output signal and the third output signal(col. 6 lines 53-55).

Re claim 23, the method of claim 22 wherein the first output signal comprises a recovered data signal (col. 4 lines 63-67).

27. The method of claim 26 wherein the third output signal comprises a recovered data signal(col. 4 lines 63-67, Moriuchi).

Re claim 33, Moriuchi discloses an integrated retimer and phase detector comprising:

a flip-flop (fig.4 (44)) comprising: at least one data input for receiving a binary data signal generated from a received signal (col. 4 lines 63-64, (a(n)); at least one clock input for receiving an extracted clock signal (col. 6 lines 32-35); and at least one output

for outputting a first output signal, wherein the first output signal comprises a feedback signal for a decision feedback equalizer (col. 2 lines 55-59) and a first phase detector signal for a clock recovery circuit (col. 6 lines 32-35);

a first latch comprising: at least one data input for receiving the first output signal (fig.7); at least one clock input for receiving the extracted clock signal (col. 6 lines 32-35); and at least one output for providing a second phase detector signal for the clock recovery circuit (col. 6 lines 53-55); and

a second latch comprising: at least one data input for receiving the second phase detector signal (fig.7); at least one clock input for receiving the extracted clock signal (col. 6 lines 32-35); and at least one output for providing a second output signal, wherein the second output signal comprises a third phase detector signal for the clock recovery circuit (col. 6 lines 53-55).

Re claim 34, the integrated retimer and phase detector of claim 33 wherein the second output signal comprises a second feedback signal for the decision feedback equalizer (S2,col. 4 lines 54-56).

Re claim 40, Moriuchi discloses a method of retiming data and generating phase detector signals (col. 4 lines 30-32), comprising:

generating a first output signal by clocking a binary data signal into a flip-flop using an extracted clock signal (col. 6 lines 32-35); providing the first output signal to a feedback loop of a decision feedback equalizer (col. 2 lines 55-59); and generating at least one phase detector output signal using the first output signal (col. 6 lines 53-55).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 12,14 rejected under 35 U.S.C. 103(a) as being unpatentable over Moriuchi US 6,556,637 in view of Mann et al. US 5,684,434

Re claim 12, Moriuchi discloses an integrated decision feedback equalizer and clock and data recovery circuit, comprising: a summer (fig.4(42)) coupled to receive an input data signal and at least one scaled feedback signal to generate a soft decision data signal (col. 2 lines 51-53); a slicer (fig.4(43)) coupled to receive the soft decision data signal to generate a binary data signal (col. 2 lines 53-55); a flip-flop (fig.4(44)) coupled to receive the binary data signal and an extracted clock signal to generate a first output signal (col. 4 lines 63-67) a plurality of latches (fig.7) coupled to receive the first output signal to generate second output signals; a voltage controlled oscillator (fig.4 (64)) coupled to receive an output signal from the loop filter to generate the extracted clock signal; and a multiplier (67) coupled to receive the first output signal to generate the at least one scaled feedback signal (col. 7 lines 2-10); does not teach a charge pump coupled to receive at least one phase detector output signal associated with the

first output signal and the second output signals; a loop filter coupled to receive an output signal from the charge pump.

However, Mann teaches a charge pump (46) coupled to receive at least one phase detector (44) output signal associated with the first output signal and the second output signals (col. 3 lines 10-14); loop filter (48) coupled to receive an output signal from the charge pump (col. 3 lines 16-17).

Therefore, taking the combined teaching of Mann and Moriuchi as a whole would have been rendered obvious to one skilled in the art to modify Mann to utilize a charge pump, loop filter coupled to receive an output signal from the charge pump for the benefit of obtaining and recovering and phase looped signal.

Re claim 14 the modified invention as claimed in claim 12 comprising at least one multiplier (67) coupled to receive at least a portion of the second output signals to generate the at least one scaled feedback signal (col. 7 lines 2-10, Moriuchi).

9. Claims 16,17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriuchi US 6,556,637 in view Cao US 2001/0033407 and further in view of in view of Mann et al. US 5,684,434

Re claim 16, Moriuchi discloses an integrated decision feedback equalizer and clock and data recovery circuit, comprising: a summer (fig.4(42)) coupled to receive an

input data signal and a plurality of scaled feedback signals to generate a soft decision data signal col. 2 lines 51-53); a slicer (fig.4(43)) coupled to receive the soft decision data signal to generate a binary data signal (col. 2 lines 53-55); a flip-flop (fig.4(44)) coupled to receive the binary data signal and an extracted clock signal to generate a first output signal (col. 4 lines 63-67, Moriuchi); a first latch (fig.7, latches connected in series) coupled to receive the first output signal to generate a second output signal; a second latch coupled to receive the second output signal to generate a third output signal (col. 6 lines 24-28); does not teach an XOR circuit coupled to receive the binary data signal, the first output signal, the second output signal and the third output signal to generate at least one phase detector output signal.

However, Cao wherein the clock recovery circuit (fig.3) comprises an XOR circuit (360,340) coupled to receive the binary data signal (para#35 lines 10-12), the first phase detector signal and at the second phase detector signals to generate at least one phase detector output signal (para#34 lines 10-14); a charge pump coupled to receive the at least one phase detector output signal; a loop filter coupled to receive an output signal from the charge pump; a voltage controlled oscillator coupled to receive an output signal from the loop filter to generate the extracted clock signal; and a plurality of multipliers coupled to receive the first output signal and the third output signal to generate the scaled feedback signals.

However, Mann teaches charge pump (46) coupled to receive at least one phase detector (44) to receive the at least one phase detector output signal (col. 3 lines 10-14); a loop filter (48) coupled to receive an output signal from the charge pump (col. 3

lines 16-17); and a voltage controlled oscillator (50) coupled to receive an output signal from the loop filter to generate the extracted clock signal (col. 3 lines 21-26).T

Therefore, taking the combined teaching of Cao and Moriuchi as a whole would have been rendered obvious to one skilled in the art to modify Moriuchi to utilize a XOR circuit coupled to receive the binary data signal, the first phase detector signal and the second phase detector signals to generate at least one phase detector output signal. for the benefit of operating a linear full rate PLL at a high frequency.

Therefore, taking the combined teaching of Cao, Moriuchi and Mann as a whole would have been rendered obvious to one skilled in the art to modify Cao and Moriuchi to utilize a charge pump, loop filter coupled to receive an output signal from the charge pump for the benefit of obtaining and recovering and phase looped signal.

Re claim 17, the modified invention as claimed in claim 16 wherein the third output signal comprises a recovered data signal (col. 4 lines 63-67, Moriuchi).

10. Claims 4,24,36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriuchi US 6,556,637 in view of Cao US 2001/0033407

Re claim 4, the integrated decision feedback equalizer and clock and data recovery circuit of claim 3 does not teach wherein the clock recovery circuit comprises an XOR circuit coupled to receive the binary data signal, the first phase detector signal

and the second phase detector signals to generate at least one phase detector output signal.

However, Cao wherein the clock recovery circuit (fig.3) comprises an XOR circuit (360) coupled to receive the binary data signal (para#35 lines 10-12), the first phase detector signal and the second phase detector signals to generate at least one phase detector output signal (para#34 lines 10-14).

Therefore, taking the combined teaching of Cao and Moriuchi as a whole would have been rendered obvious to one skilled in the art to modify Moriuchi to utilize a XOR circuit coupled to receive the binary data signal, the first phase detector signal and the second phase detector signals to generate at least one phase detector output signal. for the benefit of operating a linear full rate PLL at a high frequency.

Re claim 24, the method of claim 22 does not teach comprising generating at least one input signal for a charge pump by XORing pairs of signals selected from the group consisting of the binary data signal, the first output signal, the second output signal and the third output signal.

However, Cao discloses an XOR circuit (360,340) coupled to receive the binary data signal (para#35 lines 10-12), selected from the group consisting of the binary data signal, the first output signal, the second output signal and the third output signal. (para#34 lines 10-14).

Therefore, taking the combined teaching of Cao and Moriuchi as a whole would have been rendered obvious to one skilled in the art to modify Moriuchi to utilize a XOR

circuit coupled to receive the binary data signal, the first phase detector signal and the second phase detector signals to generate at least one phase detector output signal. for the benefit of operating a linear full rate PLL at a high frequency.

Re claim 36, the integrated retimer and phase detector of claim 33 does not teach wherein the clock recovery circuit comprises an a plurality of XOR circuit coupled to receive the binary data signal, the first phase detector signal and at least the second phase detector signals to generate at least one phase detector output signal.

However, Cao wherein the clock recovery circuit (fig.3) comprises an XOR circuit (360,340) coupled to receive the binary data signal (para#35 lines 10-12), the first phase detector signal and at the second phase detector signals to generate at least one phase detector output signal (para#34 lines 10-14).

Therefore, taking the combined teaching of Cao and Moriuchi as a whole would have been rendered obvious to one skilled in the art to modify Moriuchi to utilize a XOR circuit coupled to receive the binary data signal, the first phase detector signal and the second phase detector signals to generate at least one phase detector output signal. for the benefit of operating a linear full rate PLL at a high frequency.

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriuchi US 6,556,637 in view of Mann et al. US 5,684,434 and in further view of Cao US 2001/0033407

Re claim 13, the modified invention as claimed in claim 12 does not teach wherein the clock recovery circuit comprises an a plurality of XOR circuit coupled to receive the binary data signal, the first phase detector signal and at least the second phase detector signals to generate at least one phase detector output signal.

However, Cao wherein the clock recovery circuit (fig.3) comprises an XOR circuit (360,340) coupled to receive the binary data signal (para#35 lines 10-12), the first phase detector signal and at the second phase detector signals to generate at least one phase detector output signal (para#34 lines 10-14).

Therefore, taking the combined teaching of Moriuchi, Mann and Cao as a whole would have been rendered obvious to one skilled in the art to modify Moriuchi and Mann to utilize a XOR circuit coupled to receive the binary data signal, the first phase detector signal and the second phase detector signals to generate at least one phase detector output signal for the benefit of operating a linear full rate PLL at a high frequency.

12. Claims 5,6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriuchi US 6,556,637 in view of Cao US 2001/0033407 and in further view of Mann et al. US 5,684,434

Re claim 5, the modified invention as claimed in claim 4 does not teach wherein the clock recovery circuit comprises a charge pump coupled to receive the at least one phase detector output signal.

However, Mann teaches wherein the clock recovery circuit comprises a charge pump (46) coupled to receive at least one phase detector (44) to receive the at least one phase detector output signal (col. 3 lines 10-14).

Therefore taking the combined teaching of Cao, Moriuchi and Mann as a whole would have been rendered obvious to one skilled in the art to modify Cao and Moriuchi to utilize a charge pump, loop filter coupled to receive an output signal from the charge pump for the benefit of obtaining and recovering and phase looped signal.

Re claim 6, the modified invention as claim in claim 5 wherein the clock recovery circuit comprises: a loop filter (48) coupled to receive an output signal from the charge pump (col. 3 lines 16-17); and a voltage controlled oscillator (50) coupled to receive an output signal from the loop filter to generate the extracted clock signal (col. 3 lines 21-26,Mann).

13. Claims 11,25 rejected under 35 U.S.C. 103(a) as being unpatentable over Moriuchi US 6,556,637 in view of Shimizu et al. US 4,469,438

Re claim 11, the integrated decision feedback equalizer and clock and data recovery circuit of claim 3 discloses the extracted clock signal clocks the flip-flop and the latches (col. 6 lines 31-32) does not teach at least two of the latches are clocked by different polarities of the extracted clock signal.

However, Shimizu teaches at least two of the latches (13_1-13_n) are clocked by different polarities (fig.2) of the extracted clock signal (col. 3 lines 8-16).

Re claim 25, the modified invention as claimed in claim 22 does not teach wherein the first latch and the second latch are clocked by different polarities of the extracted clock signal.

However, Shimizu teaches first latch and the second latch (13_1-13_2) are clocked by different polarities (fig.2) of the extracted clock signal (col. 3 lines 8-16).

Therefore taking the combined teaching of Moriuchi and Shimizu as a whole would have been rendered obvious to one skilled in the art to modify Moriuchi to utilize wherein the first latch and the second latch are clocked by different polarities of the extracted clock signal for the benefit of obtaining and recovering and phase looped signal.

Re claim 35, the integrated retimer and phase detector of claim 33 does not teach wherein the first latch and the second latch are clocked by different polarities of the extracted clock signal.

However, Shimizu teaches first latch and the second latch (13_1-13_2) are clocked by different polarities (fig.2) of the extracted clock signal (col. 3 lines 8-16).

Therefore taking the combined teaching of Moriuchi and Shimizu as a whole would have been rendered obvious to one skilled in the art to modify Moriuchi to utilize wherein the first latch and the second latch are clocked by different polarities of the extracted clock signal for the benefit of obtaining and recovering and phase looped signal.

14. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriuchi US 6,556,637 in view of Mann et al. US 5,684,434 in further view of Shimizu et al. US 4,469,438

Re claim 15, the modified invention as claimed in claim 12 discloses the extracted clock signal clocks the flip-flop and the latches (col. 6 lines 31-32) does not teach at least two of the latches are clocked by different polarities of the extracted clock signal.

However, Shimizu teaches at least two of the latches (13_1-13_n) are clocked by different polarities (fig.2) of the extracted clock signal (col. 3 lines 8-16).

Therefore taking the combined teaching of Shimizu, Moriuchi and Mann as a whole would have been rendered obvious to one skilled in the art to modify Moriuchi and Mann to utilize wherein the first latch and the second latch are clocked by different polarities of the extracted clock signal for the benefit of obtaining and recovering and phase looped signal.

15. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriuchi US 6,556,637 in view Cao US 2001/0033407 further in view of in view of Mann et al. US 5,684,434 and in further view of Shimizu et al. US 4,469,438

Re claim 18, the modified invention as claimed in claim 16 wherein: the extracted clock signal clocks the flip-flop (col. 6 lines 31-32), the first latch and the second latch(fig.7); does not teach the first latch and the second latch are clocked by different polarities of the extracted clock signal.

However, Shimizu teaches first latch and the second latch (13_1-13_2) are clocked by different polarities (fig.2) of the extracted clock signal (col. 3 lines 8-16).

Therefore taking the combined teaching of Shimizu, Moriuchi, Cao and Mann as a whole would have been rendered obvious to one skilled in the art to modify combined invention of Moriuchi, Cao and Mann to utilize wherein the first latch and the second latch are clocked by different polarities of the extracted clock signal for the benefit of obtaining and recovering and phase looped signal.

Allowable Subject Matter

16. Claims 8,19-21, 37-39, 41-47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rahel Guarino whose telephone number is (571)270-1198. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Payne David can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Rahel Guarino/
Examiner, Art Unit 2611

/David C. Payne/
Supervisory Patent Examiner, Art Unit 2611